

UNITED STATES PATENT APPLICATION

FOR

SCR DEVICES IN SILICON-ON-INSULATOR CMOS

PROCESS FOR ON-CHIP ESD PROTECTION

BY

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## DESCRIPTION OF THE INVENTION

### Field of the Invention

[001] This invention pertains in general to a semiconductor device and, more particularly, to an electrostatic discharge protection circuit incorporating a silicon controlled rectifier in a silicon-on-insulator semiconductor device.

### Background of the Invention

[002] Recent advances in integrated circuits have included further development of a silicon-on-insulator (SOI) technology. An SOI technology uses an insulating substrate to improve process characteristics such as speed and latch-up susceptibility. There are two types of SOI processes, fully-depleted and partially-depleted.

[003] In an SOI complementary metal-oxide semiconductor (CMOS) technology, an independent and isolated n-type metal-oxide semiconductor (NMOS) transistor may be provided next to a p-type MOS (PMOS) transistor, and vice versa, because the NMOS and PMOS transistors are electrically isolated from each other and from the underlying silicon substrate. The main advantage of the SOI CMOS technology includes high immunity to latch-up, low junction capacitance, and low junction leakage current. The latch-up problems can be avoided because the source and drain regions of the transistors are surrounded by an insulator. In addition, an absence of diode junctions around the source and drain regions further reduces leakage current and junction capacitances. However, the SOI CMOS technology is still susceptible to an electrostatic discharge (ESD) event due to poor thermal conductivity of the insulator, e.g., buried oxide, and the floating body effect from active devices being formed over the insulator instead of a semiconductor substrate.

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[004] An ESD event refers to a phenomenon of electrical discharge of a current (positive or negative) for a short duration during which a large amount of current is provided to an integrated circuit (IC). The large current may be built-up from a variety of sources, such as the human body. To protect ICs from an ESD event, many schemes have been implemented, including use of a silicon controlled rectifier (SCR). A feature of an SCR is its voltage-holding ability, at approximately 1 volt, in a non-epitaxial bulk CMOS process. In addition, an SCR can sustain high current and hold the voltage across the SCR at a low level, and may be implemented to bypass high current discharges associated with an ESD event.

[005] A conventional SCR device has a switching voltage of more than 30 volts in sub-micron CMOS processes, and therefore is not suitable to protect gate oxides in a sub-micron CMOS technology. Fig. 1 is a reproduction of Fig. 3 of U.S. Patent No. 5,012,317 to *Rountre*, entitled "Electrostatic Discharge Protection Circuit." *Rountre* describes a lateral SCR structure made up of a P<sup>+</sup> type region 48, an N-type well 46, a P-type layer 44, and an N<sup>+</sup> region 52. According to *Rountre*, a positive current associated with an ESD event flows through region 48 to avalanche a PN junction between well 46 and layer 44. The current flows from layer 44 to region 52 across the PN junction and ultimately to ground to protect an IC from the ESD event. However, a disadvantage of the SCR structure shown in Fig. 1 is its susceptibility to being accidentally triggered by substrate noise.

[006] In addition, the p-n-p-n path of an SCR device, such as the device shown in Fig. 1, is blocked by the insulator layer and shallow trench isolations (STIs) in ICs formed with the SOI CMOS technology. Accordingly, SCR devices have been proposed in an integrated circuit based on the SOI CMOS technology. Fig. 2 is a reproduction of Fig. 4 of U.S. Patent No. 6,015,992 to *Chatterjee*, entitled "Bistable SCR-like switch for ESD

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protection of silicon-on-insulator integrated circuits.” *Chatterjee* describes an “SCR-like switch” provided by a first transistor 42 and a second transistor 44, that are separated from each other by an insulation region 60. The bistable SCR-like device has two additional lines 62, 64 to electrically connect the separate transistors.

### SUMMARY OF THE INVENTION

[007] In accordance with the invention, there is provided an integrated circuit device that includes a semiconductor substrate, an isolation layer formed over the semiconductor substrate, and a layer of silicon material, formed over the isolation layer, including a first p-type portion, a first n-type portion contiguous with the first p-type portion, a second p-type portion contiguous with the first n-type portion, a second n-type portion contiguous with the second p-type portion, a third p-type portion contiguous with the second n-type portion, and a third n-type portion contiguous with the third p-type portion. The first, second, and third p-type portions and the first, second, and third n-type portions collectively form a rectifier, the first p-type portion and the first n-type portion form a cathode of the rectifier, and the third n-type portion and the third p-type portion form an anode of the rectifier.

[008] In yet another aspect, the second n-type portion includes the third n-type portion and the third p-type portion, each of which being spaced apart from the isolation layer.

[009] In another aspect, the second p-type portion includes a fourth n-type portion formed spaced apart from the first n-type portion, and the first n-type portion and the fourth n-type portion define a source region and a drain region of an NMOS transistor.

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[010] In still another aspect, the second n-type portion includes a fourth p-type portion formed spaced apart from the third p-type portion, and the third p-type portion and the fourth p-type portion define a source region and a drain region of a PMOS transistor.

[011] Also in accordance with the present invention, there is provided an integrated circuit device that includes a semiconductor substrate, an isolation layer formed over the semiconductor substrate, an n-type MOS transistor having a gate, a drain region, and a source region formed over the isolation layer, and a p-type MOS transistor having a gate, a drain region, and a source region formed over the isolation layer and contiguous with the n-type MOS transistor, wherein the n-type MOS transistor and the p-type MOS transistor form a rectifier to provide electrostatic discharge protection.

[012] In another aspect, the integrated circuit device further comprises an electrostatic discharge circuit for providing the bias voltage to trigger the rectifier. The electrostatic discharge circuit comprising a first inverter including a first PMOS transistor having a gate, a source region and a drain region, and a first NMOS transistor having a gate, a source region and a drain region, wherein the gate of the first PMOS transistor is coupled to the gate of the first NMOS transistor, and the gate of the p-type MOS transistor is coupled to the drain region of the first PMOS transistor and the drain region of the first NMOS transistor.

[013] In yet another aspect, the electrostatic discharge circuit further comprises a second inverter, including a second PMOS transistor having a gate, a source region and a drain region, and a second NMOS transistor having a gate, a source region and a drain region, wherein the gate of the second PMOS transistor is coupled to the gate of the second

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NMOS transistor, and the gate of the n-type MOS transistor is coupled to the drain region of the second PMOS transistor and the drain region of the second NMOS transistor.

[014] In still another aspect, the cathode is coupled to at least one diode to prevent the rectifier from being triggered in a non-ESD operation.

[015] Further in accordance with the present invention, there is provided a method for protecting a silicon-on-insulator semiconductor circuit from electrostatic discharge that includes providing an n-type MOS transistor having a source region and a drain region in the silicon-on-insulator circuit, providing a p-type MOS transistor having a source region and a drain region, the p-type MOS transistor being contiguous with the n-type MOS transistor, providing a p-type region contiguous with one of the source region and the drain region of the n-type MOS transistor to form a cathode, and providing an n-type region contiguous with one of the source region and the drain region of the p-type MOS transistor to form an anode, wherein the n-type region, the p-type region, the p-type MOS transistor and the n-type MOS transistor form a rectifier.

[016] Additional objects and advantages of the invention will be set forth in part in the description which follows, and in part will be obvious from the description, or may be learned by practice of the invention. The objects and advantages of the invention will be realized and attained by means of the elements and combinations particularly pointed out in the appended claims.

[017] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory only and are not restrictive of the invention, as claimed.

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[018] The accompanying drawings, which are incorporated in and constitute a part of this specification, illustrate several embodiments of the invention and together with the description, serve to explain the principles of the invention.

### **BRIEF DESCRIPTION OF THE DRAWINGS**

[019] Figure 1 is a cross-sectional view of a known silicon controlled rectifier;

[020] Figure 2 is a cross-sectional view of another known silicon controlled rectifier;

[021] Figure 3 is a cross-sectional view of an SCR structure in accordance with an embodiment of the present invention;

[022] Figure 4 is a perspective view of the SCR structure shown in Figure 3;

[023] Figure 5 is a cross-sectional view of an SCR structure in accordance with another embodiment of the present invention;

[024] Figure 6 is a perspective view of the SCR structure shown in Figure 5;

[025] Figure 7A is a circuit block diagram showing an embodiment for implementing the SCR structure shown in Figures 3 and 5;

[026] Figure 7B is a detailed circuit diagram of Figure 7A;

[027] Figure 8A is a circuit block diagram showing another embodiment for implementing the SCR structure shown in Figures 3 and 5; and

[028] Figure 8B is a detailed circuit diagram of Figure 8A;

### **DESCRIPTION OF THE EMBODIMENTS**

[029] Reference will now be made in detail to the present exemplary embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever

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possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

[030] The present invention provides a silicon controlled rectifier (SCR) structure to protect an integrated circuit, manufactured using a SOI CMOS technology, from an ESD event. The SCR structure of the present invention includes an NMOS transistor and a PMOS transistor, each of which may be triggered by an optional detection circuit, and may employ polysilicon gates to block STI regions to provide compact SCR structures. In addition, the SCR structures of the present invention may be controlled for improved trigger speed, which, in turn, provides improved ESD protection.

[031] Figure 3 is a cross-sectional view of an SCR structure of an embodiment consistent with the present invention and formed using a partially-depleted SOI CMOS process. Referring to Figure 3, an integrated circuit device includes a semiconductor substrate 100. In the present embodiment, semiconductor substrate 100 is a p-type substrate. An isolation, or insulation, layer 102, such as a buried oxide, is formed over semiconductor substrate 100. A layer of silicon material (not numbered) is formed over isolation layer 102 and includes a p-well 106 and an n-well 108 contiguous with p-well 106. Both p-well 106 and n-well 108 are lightly doped regions defined by a diffusion process. A junction is formed between P-well 106 and n-well 108.

[032] A heavily-doped first p-type portion 110 and a heavily-doped first n-type portion 112 are formed in p-well 106 and spaced apart from isolation layer 102. In other words, neither first p-type portion 110 nor first n-type portion 112 is contiguous with isolation layer 102. A junction is formed between first n-type portion 112 and p-well 106. First p-type portion 110 has a doping concentration higher than that of p-well 106. A

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heavily-doped second p-type portion 116 and a heavily-doped second n-type portion 114 are formed inside n-well 108 and spaced apart from isolation layer 102. A junction is formed between second p-type portion 116 and n-well 108. Second n-type portion 114 has a doping concentration higher than that of n-well 108. First n-type portion 112, p-well 106, n-well 108, second p-type portion 116, and second n-type portion 114 collectively form an SCR structure consistent with the present invention. First p-type portion 110 and first n-type portion 112 form a cathode 138 of the SCR structure, and second p-type portion 116 and second n-type portion 114 form an anode 140 of the SCR structure. Each of cathode 138 and anode 140 receives an ESD current.

[033] A third n-type portion 142 is formed in p-well 106 and spaced apart from first n-type portion 112, wherein each of first n-type portion 112 and third n-type portion 142 define one of a source region or a drain region of an NMOS transistor (not numbered). The NMOS transistor may further include a fourth n-type portion 118 and a fifth n-type portion 120. Specifically, first n-type portion 112 has a doping concentration higher than that of fourth n-type portion 118, and together form one of the source and drain regions of the NMOS transistor. Third n-type portion 142 has a doping concentration higher than that of fifth n-type portion 120, and together form another one of the source and drain regions of the NMOS transistor. The NMOS transistor also includes a gate oxide 122 formed over p-well 106. The NMOS transistor further includes a gate 124 provided over gate oxide 122 and between n-type regions 118 and 120, and a conducting polycide layer 126 formed over gate 124. Sidewall spacers (not numbered) are formed on the sides of gate 124.

[034] Similarly, a third p-type portion 144 is formed in n-well 108 and spaced apart from second p-type portion 116, wherein second p-type portion 116 and third p-type

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portion 144 define a source region and a drain region of a PMOS transistor (not numbered). The PMOS transistor may further include a fourth p-type portion 128 and a fifth p-type portion 130. Specifically, third p-type portion 144 has a doping concentration higher than that of fourth p-type portion 128, and together form one of the source and drain regions of the PMOS transistor. Second p-type portion 116 has a doping concentration higher than that of fifth p-type portion 130, and together form another one of the source and drain regions of the PMOS transistor. The PMOS transistor also includes a gate oxide 132 formed over n-well 108. The PMOS transistor additionally includes a gate 134 provided over gate oxide 132 and between p-type regions 128 and 130, and a polycide 136 is formed over gate 134. Sidewall spacers (not numbered) are formed on the sides of gate 134. Shallow trench isolations (STIs) 104 are formed over isolation layer 102 and contiguous with the SCR structure.

[035] In operation, when a positive transient voltage is received at anode 140, the SCR structure shown in Fig. 3 turns on to conduct the transient current to cathode 138. The transient current flows from anode 140 to p-type portion 116 and then n-well 108. The transient current then flows from n-well 108 to p-well 106, and then across the junction between p-well 106 and n-type portion 112 to cathode 138.

[036] When a negative transient voltage is received at cathode 138, the SCR structure turns on to conduct the transient current to anode 140. The negative transient current flows from cathode 138 to n-type portion 112 and then p-well 106. The transient current then flows from p-well 106 to n-well 108, and then to p-type portion 116 and anode 140.

[037] Providing an appropriate voltage to gate 124 would turn on the NMOS transistor of the SCR, and the NMOS transistor is triggered to conduct a current flow from

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third n-type portion 142 to n-type portion 112. Likewise, the PMOS transistor of the SCR structure could be turned on by providing an appropriate voltage to gate 134 and, as a result, the PMOS transistor is triggered to conduct a current flow in the direction from p-type portion 116 to n-type portion 114. Either the NMOS transistor or the PMOS transistor having being turned on causes forward biasing of the SCR structure, which turns on the SCR structure.

[038] Figure 4 is a perspective view of the SCR structure shown in Figure 3. For illustrative purposes, the upper interconnect layers are not shown. Referring to Figure 4, a p-type substrate 100 is provided with a layer of isolation layer 102 disposed over substrate 100. Isolation layer 102 may be an implanted layer formed according to any known SOI CMOS technology. A layer of silicon material (not numbered) is then formed over isolation layer 102. Active circuits are formed on or in the silicon material. As such, the active circuits are isolated from the substrate and may be insulated laterally with STIs 104.

[039] Figure 5 is a cross-sectional view of an SCR structure in accordance with another embodiment consistent with the present invention and formed in a fully-depleted SOI CMOS process. Referring to Figure 5, an integrated circuit device includes a semiconductor substrate 200. In the present embodiment, semiconductor substrate 200 is a p-type substrate. An isolation, or insulation, layer 202, such as a buried oxide, is formed over semiconductor substrate 200. A layer of silicon material (not numbered) is formed over isolation layer 202 and includes a p-well 210 and an n-well 216 contiguous with p-well 210. Both p-well 210 and n-well 216 are lightly-doped regions defined by a diffusion process. A junction is formed between P-well 210 and n-well 216.

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[040] A heavily-doped first p-type portion 206 is formed over isolation layer 202.

A heavily-doped first n-type portion 208 is formed over isolation layer 202 and contiguous with first p-type portion 206 and p-well 210. A junction is formed between first n-type portion 208 and p-well 210. First p-type portion 206 has a doping concentration higher than that of p-well 210. A heavily-doped second n-type portion 220 is formed over isolation layer 202. A heavily-doped second p-type portion 218 is formed over isolation layer 202 and contiguous with second n-type portion 220 and n-well 216. A junction is formed between second p-type portion 218 and n-well 216. Second n-type portion 220 has a doping concentration higher than that of n-well 216. First p-type portion 206, first n-type portion 208, p-well 210, n-well 216, second p-type portion 218, and second n-type portion 220 collectively form an SCR structure consistent with the present invention. First p-type portion 206 and first n-type portion 208 form a cathode 234 of the SCR structure, and second p-type portion 218 and second n-type portion 220 form an anode 236 of the SCR structure. Each of cathode 234 and anode 236 receives an ESD current.

[041] A third n-type portion 212 is formed in p-well 210 and spaced apart from first n-type portion 208, wherein each of the first n-type portion 208 and third n-type portion 212 define a source region or a drain region of an NMOS transistor (not numbered). The NMOS transistor also includes a gate oxide 222 formed over p-well 210. The NMOS transistor further includes a gate 224 provided over gate oxide 222 and between n-type regions 208 and 212, and a conducting polycide layer 226 is formed over gate 224.

[042] Similarly, a third p-type portion 214 is formed in n-well 216 and spaced apart from second p-type portion 218, wherein each of the second p-type portion 218 and third p-type portion 214 define a source region or a drain region of a PMOS transistor (not

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numbered). The PMOS transistor also includes a gate oxide 228 formed over n-well 216.

The PMOS transistor additionally includes a gate 230 provided over gate oxide 222 and between p-type regions 218 and 214, and a polycide layer 232 is formed over gate 230.

Shallow trench isolations (STIs) 204 are formed over isolation layer 202 and contiguous with the SCR structure. The SCR structure shown in Figure 5 operates in the same manner as the SCR device shown in Figure 3.

[043] Figure 6 is a perspective view of the SCR structure shown in Figure 5. For illustrative purposes, the upper interconnect layers are not shown. Referring to Figure 6, a p-type substrate 200 is provided with a layer of isolation layer 202 disposed over substrate 200. Isolation layer 202 may be an implanted layer formed according to any known SOI CMOS technology. A layer of silicon material (not numbered) is then deposited over isolation layer 202. Active circuits are formed on or in the silicon material. As such, the active circuits are isolated from the substrate and may be insulated laterally with STIs 204.

[044] Figure 7A is a circuit block diagram showing an embodiment for implementing the SCR structure shown in Figures 3 and 5 to provide ESD protection. Referring to Figure 7A, an SCR device 300 having the structure shown in Figure 3 is conceptually represented as a four-terminal device, having anode 140, cathode 138, gate 134 of its PMOS transistor (not shown), and gate 124 of its NMOS transistor (not shown). Anode 140 is coupled to a pad 302, and cathode 138 is coupled to ground. Each of gates 134 and 124 is coupled to an ESD detecting circuit 304, which operates to reduce the turn-on time of SCR device 300. Up occurrence of an ESD event, ESD detecting circuit 304 detects an ESD transient pulse on pad 302 and provides a bias voltage to one or both of gates 134 and 124 to trigger SCR device 300 to discharge ESD current.

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[045] Figure 7B is a detailed circuit diagram of Figure 7A. Referring to Figure 7B, ESD detecting circuit 304 includes a first transistor-pair including a PMOS transistor 306 having a gate 306-1, a source region 306-3 and a drain region 306-2, and an NMOS transistor 308 having a gate 308-1, a source region 308-3 and a drain region 308-2. Gate 306-1 of PMOS transistor 306 is coupled to gate 308-1 of NMOS transistor 308. Gate 134 is coupled at a node 330 to drain region 306-2 of PMOS transistor 306 and drain region 308-2 of NMOS transistor 308. Source 306-3 of PMOS transistor 306 is coupled to pad 302 and anode 140 of the SCR device 300. Source 308-3 of NMOS transistor 308 is coupled to ground.

[046] ESD detecting circuit 304 also includes a second transistor-pair including a PMOS transistor 310 having a gate 310-1, a source region 310-3 and a drain region 310-2, and an NMOS transistor 312 having a gate 312-1, a source region 312-3 and a drain region 312-2. Gate 310-1 of PMOS transistor 310 is coupled to gate 312-1 of NMOS transistor 312. Gate 124 is coupled at a node 332 to drain region 310-2 of PMOS transistor 310, drain region 312-2 of the NMOS transistor 312, gate 306-1 of PMOS transistor 306, and gate 308-1 of NMOS transistor 308. Source 310-3 of PMOS transistor 310 is coupled to pad 302, anode 140 of the SCR device 300, and source 306-3 of PMOS transistor 306. Source 312-3 of NMOS transistor 312 is coupled to ground.

[047] ESD detecting circuit 304 further includes a resistor 314 and a capacitor 316. Resistor 314 is coupled to pad 302 at one end, and at a node 334 coupled to gate 310-1 of PMOS transistor 310, and gate 312-1 of NMOS transistor 312, and capacitor 316 at the other end. Capacitor 316 is coupled between node 334 and ground.

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[048] In operation, each of the first and second transistor-pairs functions as inverters. In normal operation, node 334 is at a high voltage level, and one of the inverters functions to provide a low voltage at node 332. Therefore, a low voltage is provided to gate 124 of the NMOS transistor to keep the NMOS transistor off so that SCR device 300 remains off. Likewise, the other one of the inverters functions to provide a high voltage to node 330. Thus, a high voltage is provided to gate 134 of the PMOS transistor to keep the PMOS transistor off so that SCR device 300 remains off.

[049] In an ESD event, a positive ESD pulse is presented across VDD-VSS power rails. Therefore, in response to the positive pulse, node 334 is initially at a low voltage level, which is inverted into a high voltage level at node 332. This high voltage level is provided to gate 124 of the NMOS transistor to turn on the NMOS transistor, which triggers the SCR device 300. The high voltage level at node 332 is inverted by the first transistor pair to a low voltage level at node 330 to turn on the PMOS transistor of SCR device 300. As a result, SCR device 300 is turned on and conducts to bypass the ESD current. When both the PMOS and NMOS transistors of the SCR device 300 are turned on, the reaction time to turn on the SCR device 300 is significantly reduced.

[050] Figure 8A is a circuit block diagram showing another embodiment for implementing the SCR structure shown in Figure 3 to provide ESD protection. Figure 8A is similar to Figure 7A, except that it includes an ESD detecting circuit 304', that SCR device 300 is coupled across VDD-VSS power rails, and that cathode 138 of SCR device 300 is coupled to a plurality of serially connected diodes D1 . . . Dn. Diode D1 is coupled to cathode 138 and diode Dn is coupled to ground, i.e., the VSS power rail. In one embodiment, cathode 138 of SCR device 300 is coupled to a single diode.

[051] Figure 8B is a detailed circuit diagram of Figure 8A. Referring to Figure 8B, ESD detecting circuit 304' includes an inverter having a transistor-pair, including a PMOS transistor 318 having a gate 318-1, a source region 318-3 and a drain region 318-2, and an NMOS transistor 320 having a gate 320-1, a source region 320-3 and a drain region 320-2. Gate 318-1 of PMOS transistor 318 is coupled to gate 320-1 of NMOS transistor 320. Gate 124 of SCR device 300 is coupled at node 336 to drain region 318-2 of PMOS transistor 318 and drain region 320-2 of the NMOS transistor 320. Source 318-3 of PMOS transistor 318 is coupled to VDD, as is anode 140 of SCR device 300. Source 320-3 of NMOS transistor 320 is coupled to VSS. Gate 134 of SCR device 300 is coupled to anode 140 through a resistor 326, which functions to protect the gate oxide layer of the PMOS transistor.

[052] ESD detecting circuit 304' further includes a resistor 322 and a capacitor 324. Resistor 322 is coupled to VDD at one end, and at node 338 coupled to gate 318-1 of PMOS transistor 318, gate 320-1 of NMOS transistor 320, and capacitor 324 at the other end. Capacitor 324 is coupled between node 338 and VSS.

[053] In operation, diodes D1 . . . Dn function to raise a holding voltage when SCR device 300 is triggered. The holding voltage must be higher than the voltage drop across the VDD-VSS power rails to avoid latch-up. In addition, the diodes prevent SCR device 300 from being latched-up if accidentally triggered by a noise signal during normal operation.

[054] In normal operation, i.e., in the absence of an ESD event, node 338 is at a high voltage level, and the inverter functions to provide a low voltage at node 336.

Therefore, a low voltage is provided to gate 124 of the NMOS transistor to keep the NMOS



transistor off so that SCR device 300 remains off. Because gate 134 of the PMOS transistor is coupled to anode 140 and VDD, the PMOS transistor remains off, as does SCR device 300. During an ESD event, a positive ESD pulse is presented across the VDD-VSS power rails. Node 338 is, therefore, at a low voltage level, and through the inverter, a high voltage level is presented at node 336, which turns on the NMOS transistor of the SCR device 300. The SCR device 300 conducts to allow the ESD current to flow through the n-well of the NMOS transistor, producing a voltage drop. The ESD current is discharged from the VDD-VSS power rails through the SCR device 300 and diodes D1 . . . Dn.

[055] Embodiments consistent with the present invention also provide a method for protecting a silicon-on-insulator semiconductor circuit from electrostatic discharge. The method includes providing an n-type MOS transistor having a source region and a drain region in the silicon-on-insulator circuit, providing a p-type MOS transistor having a source region and a drain region, the p-type MOS transistor being contiguous with the n-type transistor, providing a p-type region contiguous with one of the source region and the drain region of the n-type MOS transistor to form a cathode, and providing an n-type region contiguous with one of the source region and the drain region of the p-type MOS transistor to form an anode, wherein the n-type region, the p-type region, the p-type MOS transistor and the n-type MOS transistor form an SCR structure. The method of the present invention may also include biasing the p-type MOS transistor to trigger the SCR structure and biasing the n-type MOS transistor to trigger the SCR structure.

[056] Other embodiments of the invention will be apparent to those skilled in the art from consideration of the specification and practice of the invention disclosed herein. It is

Country	Year	Population (millions)	Urban population (millions)	Urban population (%)	Population density (per sq. km)	Urban population density (per sq. km)
Algeria	1975	10.5	4.5	42.9	10.5	10.5
Algeria	1980	11.5	5.5	47.8	11.5	11.5
Algeria	1985	12.5	6.5	51.6	12.5	12.5
Algeria	1990	13.5	7.5	55.5	13.5	13.5
Algeria	1995	14.5	8.5	58.6	14.5	14.5
Algeria	2000	15.5	9.5	61.3	15.5	15.5
Algeria	2005	16.5	10.5	63.6	16.5	16.5
Algeria	2010	17.5	11.5	65.7	17.5	17.5
Algeria	2015	18.5	12.5	67.6	18.5	18.5
Algeria	2020	19.5	13.5	69.2	19.5	19.5
Algeria	2025	20.5	14.5	70.7	20.5	20.5
Algeria	2030	21.5	15.5	72.1	21.5	21.5
Algeria	2035	22.5	16.5	73.3	22.5	22.5
Algeria	2040	23.5	17.5	74.5	23.5	23.5
Algeria	2045	24.5	18.5	75.5	24.5	24.5
Algeria	2050	25.5	19.5	76.5	25.5	25.5
Algeria	2055	26.5	20.5	77.4	26.5	26.5
Algeria	2060	27.5	21.5	78.2	27.5	27.5
Algeria	2065	28.5	22.5	78.9	28.5	28.5
Algeria	2070	29.5	23.5	79.7	29.5	29.5
Algeria	2075	30.5	24.5	80.3	30.5	30.5
Algeria	2080	31.5	25.5	81.0	31.5	31.5
Algeria	2085	32.5	26.5	81.6	32.5	32.5
Algeria	2090	33.5	27.5	82.1	33.5	33.5
Algeria	2095	34.5	28.5	82.6	34.5	34.5
Algeria	2100	35.5	29.5	83.1	35.5	35.5
Algeria	2105	36.5	30.5	83.6	36.5	36.5
Algeria	2110	37.5	31.5	84.0	37.5	37.5
Algeria	2115	38.5	32.5	84.4	38.5	38.5
Algeria	2120	39.5	33.5	84.8	39.5	39.5
Algeria	2125	40.5	34.5	85.2	40.5	40.5
Algeria	2130	41.5	35.5	85.5	41.5	41.5
Algeria	2135	42.5	36.5	85.9	42.5	42.5
Algeria	2140	43.5	37.5	86.2	43.5	43.5
Algeria	2145	44.5	38.5	86.5	44.5	44.5
Algeria	2150	45.5	39.5	86.8	45.5	45.5
Algeria	2155	46.5	40.5	86.9	46.5	46.5
Algeria	2160	47.5	41.5	87.2	47.5	47.5
Algeria	2165	48.5	42.5	87.4	48.5	48.5
Algeria	2170	49.5	43.5	87.7	49.5	49.5
Algeria	2175	50.5	44.5	87.9	50.5	50.5
Algeria	2180	51.5	45.5	88.1	51.5	51.5
Algeria	2185	52.5	46.5	88.2	52.5	52.5
Algeria	2190	53.5	47.5	88.4	53.5	53.5
Algeria	2195	54.5	48.5	88.4	54.5	54.5
Algeria	2200	55.5	49.5	88.5	55.5	55.5
Algeria	2205	56.5	50.5	88.5	56.5	56.5
Algeria	2210	57.5	51.5	88.5	57.5	57.5
Algeria	2215	58.5	52.5	88.5	58.5	58.5
Algeria	2220	59.5	53.5	88.4	59.5	59.5
Algeria	2225	60.5	54.5	88.4	60.5	60.5
Algeria	2230	61.5	55.5	88.4	61.5	61.5
Algeria	2235	62.5	56.5	88.3	62	

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